This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

Claim 1 (Currently Amended): A system for dynamically optimizing a clock speed of a clock signal used for timing of data signal transmissions and receptions within an integrated circuit (IC) device comprising:

a transmitter means for successively transmitting data signals for receipt by a receiver device within said IC;

a clock generator circuit for providing ~~said~~ a clock timing signal to respective said transmitter means and said receiver device, said clock timing signal used for timing said data signal transmission and reception within said IC at successively different clock speeds, each said successive data signal transmission transmitted at a different clock speed;

a monitoring circuit means for receiving successive data signal transmissions generated at different clock speeds and detecting when a data signal transmission fail point is achieved at a particular clock speed; and,

means for adjusting said clock timing signal provided to respective said transmitter means and said receiver device at each clock speed, said means adjusting said clock timing signal to achieve ~~according to~~ a maximum speed allowed for the IC that avoids said data transmission fail point during real-time operation.

Claim 2 (Original): The system as claimed in Claim 1, wherein said means for adjusting comprises means for generating a feedback control signal for input to said clock generator circuit for adjusting said clock to said maximum speed.

Claim 3 (Original): The system as claimed in Claim 1, wherein said clock generator circuit comprises

a multiplexor device comprising one or more clock taps responsive to said feedback control signal for enabling alteration of said clock speed.

Claim 4 (Previously presented): The system as claimed in Claim 2, further comprising:

an error correction code signal generating circuit for generating error correction code signals according to each data signal transmission,

said monitoring circuit comprising an error correction code signal check circuit for receiving said error correction code signals and comparing error correction signals generated at each clock speed against known error corrections corresponding to each data signal transmission, wherein said data transmission fail point corresponds to a clock speed resulting in an error between said error correction code signals and said corresponding known error correction codes.

Claim 5 (Previously presented): The system as claimed in Claim 2, further comprising:

a means for delaying each of a series of data transmission signals generated at different clock speeds;

said monitoring circuit comprising an error check circuit for receiving each of said series of delayed data transmission signals and comparing each delayed data transmission signal against a corresponding known data signal transmission, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said delayed data transmission signal and said corresponding known data transmission.

Claim 6 (Currently amended): The system as claimed in Claim 2, further comprising:

a random data generating circuit for generating unique random data ~~transmission~~ signals for ~~input to~~ transmission throughout a data path of a circuit within said IC device, said ~~IC device~~ circuit for processing said random data signals ~~in~~ and generating a corresponding data output;

said monitoring circuit including a means for comparing said generated random data against said corresponding data output of said processing circuit, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said generated random data and said corresponding processing circuit output.

Claim 7 (Original): The system as claimed in Claim 6, wherein said comparator means generates said feedback control signal indicating said data output of said processing circuit matches said generated random data, said feedback control signal being input to said clock generator circuit for enabling the clock frequency provided by clock generator circuit to be increased.

Claim 8 (Original): The system as claimed in Claim 6, wherein said comparator means generates said feedback control signal indicating said data output of said processing circuit does not match said generated random data, said feedback control signal being input to said clock generator circuit for enabling the clock frequency provided by clock generator circuit to be decreased.

Claim 9 (Original): The system as claimed in Claim 6, wherein said random data generating circuit includes a random number generator for receiving a seed value and generating said unique random data therefrom.

Claim 10 (Original): The system as claimed in Claim 5, wherein said means for delaying each of a series of data transmission signals comprises means for increasing a load applied to data lines carrying said data transmission signals to said error check circuit.

Claim 11 (Currently Amended): A method for dynamically optimizing a system clock speed of a clock signal used for timing of data signal transmission and receptions in an Integrated Circuit (IC), said method comprising the steps of:

a) successively transmitting data signals for receipt by a receiver device within said IC,

b) providing said clock timing signal to respective said transmitter means and said receiver device, said clock timing signal used for timing of data signal transmission and reception within said IC at successively different clock speeds~~, each said data signal transmission transmitted at a different clock speed~~

c) receiving successive data transmissions generated at different clock speeds and detecting when a data signal transmission fail point is achieved at a particular clock speed; and,

d) adjusting said clock timing signal provided to respective said transmitter means and said receiver device at each clock speed, said clock timing signal adjusted to achieve ~~according to~~ a maximum speed allowed for the IC that avoids said data transmission fail point during real-time operation.

Claim 12 (Previously presented): The method as claimed in Claim 11, wherein said adjusting step d) includes the step of generating a feedback control signal for input to said clock generator circuit, said feedback signal for adjusting said clock to said maximum speed.

Claim 13 (Previously presented): The method as claimed in Claim 12, further comprising the steps of:

generating error correction code signals according to each data signal transmission,

receiving said error correction code signals and comparing error correction signals generated at each clock speed against known error correction codes corresponding to each data transmission, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said error correction signals and said corresponding known error correction codes.

Claim 14 (Original): The method as claimed in Claim 12, further comprising the steps of:

delaying each of a series of data transmission signals generated at different clock speeds;

receiving each of said series of delayed data transmission signals and comparing each delayed data transmission signal against its corresponding known data signal transmission, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said delayed data transmission signal and said corresponding known data transmission.

Claim 15 (Previously presented): The method as claimed in Claim 12, further comprising the steps of:

generating unique random data transmission signals;

transmitting said unique random data signals throughout a data path of a circuit within said IC device for processing therein, and generating a corresponding data output signal; and,

comparing said generated random data against said corresponding data output of said processing circuit, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said generated random data and said corresponding processing circuit output.

Claim 16 (Currently Amended): The method as claimed in Claim 12, wherein said feedback control signal includes a first signal indicating a match between said data output signal of said data path and said generated unique random data, or generating a second output signal indicating no match between said data output signal of said data path and said generated unique random data, wherein said adjusting step [[c)]] d) includes responding to either said first or second output signals for respectively increasing or decreasing a clock frequency of said clock signal.

Claim 17 (Original): The method as claimed in Claim 14, wherein said delaying step includes the step of increasing a load applied to data lines carrying said data transmission signals to said error check circuit.

Claim 18 (Original): The method as claimed in Claim 12, further including the step of continuously detecting presence of data transmission fail points to ensure that the errors do not occur as the IC incurs different operating conditions, said monitoring including adjusting the clock speed accordingly.